

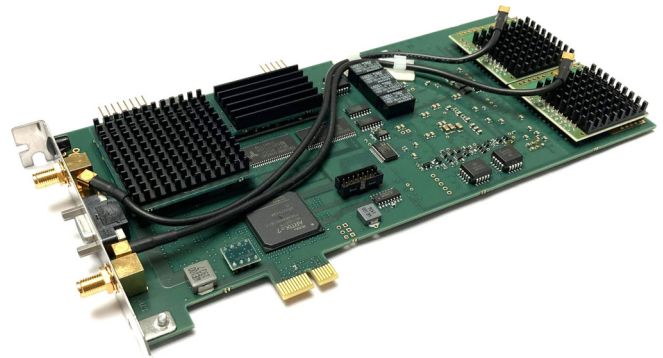


SPC-180NX

TCSPC / FLIM Module

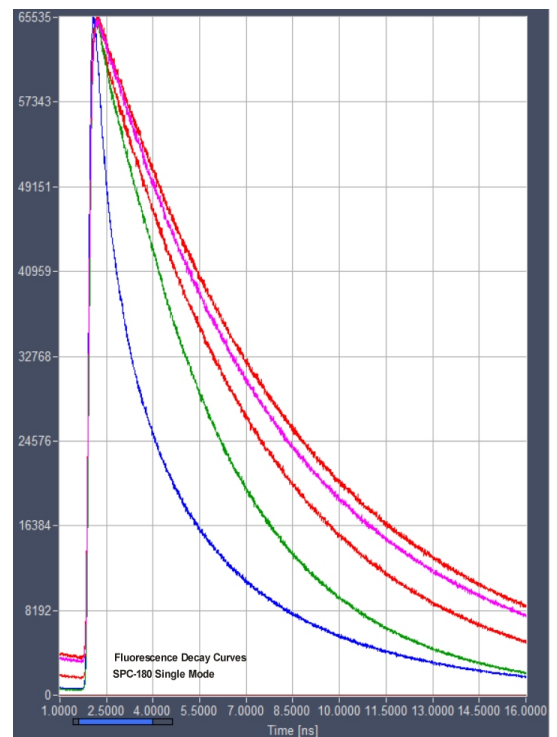
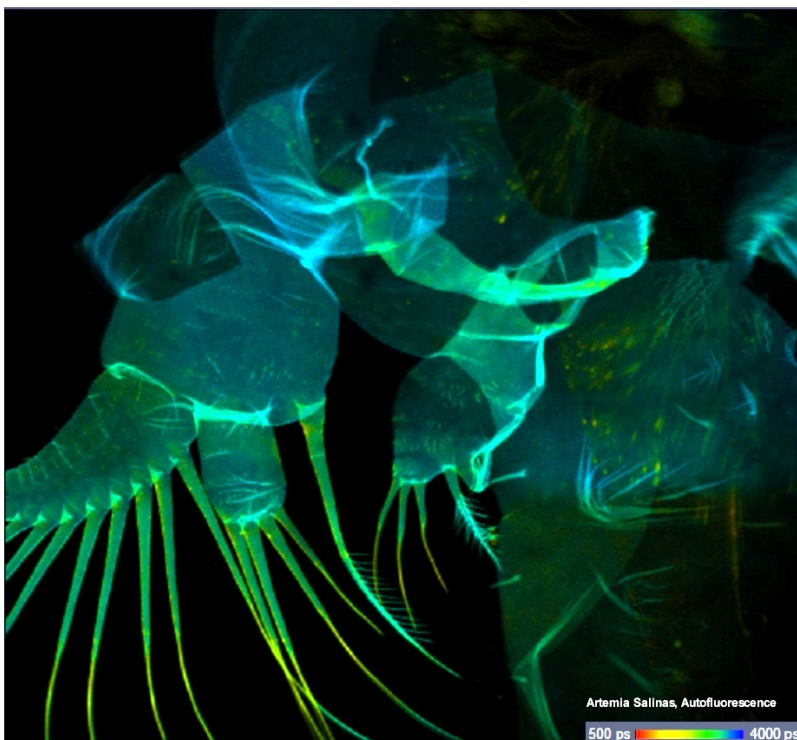
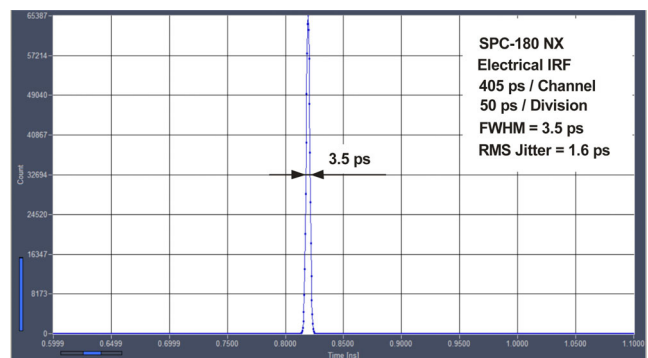
High-Resolution Time-Correlated Single Photon Counting Module

High-throughput PCI-Express interface
Ultra-fast ultra-stable timing electronics
Electrical IRF width 3.5 ps FWHM
Internal timing jitter 1.6 ps RMS
Time-channel width down to 407 fs
Discriminator input bandwidth 4 GHz
Photon distribution and parameter-tag modes
Multi-detector / multi-wavelength capability
Excitation-wavelength multiplexing
Parallel operation of 2, 3 or 4 modules
Laser repetition rates up to 150 MHz
Dead time 80 ns
Saturated count rate 12.5 MHz



Fluorescence-decay experiments
Anti-bunching experiments
Single-wavelength FLIM, multi-wavelength FLIM
Fast-acquisition FLIM
Accumulated time-series FLIM
Simultaneous FLIM / PLIM
Mosaic FLIM

Metabolic imaging
Double-exponential FRET imaging
FLIM of fast physiological processes
Recording of Ca^{2+} transients
fNIRS and NIRS experiments
Single-molecule spectroscopy
Fluorescence correlation



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SPC-180NX

TCSPC / FLIM Module

Photon Channel

Principle
 Discriminator Input Bandwidth
 IRF width, FWHM
 RMS timing jitter
 Variance in time of IRF centroid
 Optimum Input Voltage Range
 Min. Input Pulse Width
 Threshold
 Zero Cross Adjust

Constant Fraction Discriminator (CFD)
 4 GHz
 < 3.5 ps, FWHM
 < 1.6 ps, RMS
 < 0.4 ps rms over 100 seconds
 - 30 mV to - 500 mV
 200 ps
 0 to - 250 mV
 - 100 mV to + 100 mV

Synchronisation Channel

Principle
 Discriminator Input Bandwidth
 Optimal Input Voltage Range
 Min. Input Pulse Width
 Threshold
 Frequency Range
 SYNC Frequency Divider
 Zero Cross Adjust

Constant Fraction Discriminator (CFD)
 4 GHz
 - 30 mV to - 500 mV
 200 ps
 0 to -250 mV
 0 to 150 MHz
 1 - 2 - 4
 -100 mV to + 100 mV

Time-to-Amplitude Converters / ADCs

Principle
 TAC Range
 Biased Amplifier Gain
 Biased Amplifier Offset
 Time Range incl. Biased Amplifier
 min. Time / Channel
 ADC Principle
 Diff. Nonlinearity, electrical

Ramp Generator / Biased Amplifier
 25 ns to 2.5 us
 1 to 15
 0 to 50 % of TAC Range
 1.67 ns to 2.5 us
 407 fs
 50 ns Flash ADC with Error Correction
 < 0.5% rms, typ. <1% peak-peak

Data Acquisition (Histogram Modes)

Method
 Dead Time
 Saturated Count Rate
 Useful count rate
 max. Counts / Time Channel (counting depth)
 Overflow Control
 Collection Time
 Display Interval Time
 Repeat Time
 Sequential Recording
 Synchronisation with Scanning
 Routing
 Count enable
 Experiment Trigger

on-board multi-dimensional hardware histogramming process
 80 ns, independent of computer speed
 12 MHz
 6 MHz
 $2^{16}-1$
 none / stop / repeat and correct
 0.1 us to 100,000 s
 10 ms to 100,000 s
 0.1 us to 100,000 s
 Unlimited recording by memory swapping
 pixel, line and frame clocks from scanning device
 7 bit TTL
 1 bit TTL
 TTL

Data Acquisition (FIFO / Parameter-Tag Mode)

Method
 Online display
 FCS calculation
 Number of counts of decay / waveform recording
 Dead Time
 Saturated count rate, peak
 Sustained count rate (bus-transfer limited)
 max. counts / time channel (counting depth)
 Output Data Format (ADC / Macrotime / Routing)
 On-board FIFO buffer Capacity (photons)
 Macro Timer Resolution, internal clock
 Macro Timer Resolution, clock from SYNC input
 Routing
 External event markers
 Experiment trigger

Parameter-tagging of individual photons and continuous writing to disk
 Decay function, FCS, Cross-FCS, PCH, MCS traces
 Multi-tau algorithm, online calculation and online fit
 unlimited
 80 ns
 12 MHz
 5 MHz
 unlimited
 12 / 12 / 4 bit
 $2 \cdot 10^6$
 25 ns, 12 bit, overflows marked by MTOF entry in data stream
 10 ns to 100 ns, 12 bit, overflows marked by MTOF entry in data stream
 4 bit TTL
 4 bit, TTL
 TTL

Data Acquisition, FIFO Imaging

Method
 Online display
 Synchronisation with scanner
 Detector / Wavelength Channels
 Image resolution, 64-bit SPCM software
 No of time channels
 No. of pixels, 1 detector channel
 No. of pixels, 16 detector channels

Buildup of images from time- and wavelength tagged data
 up to 8 images in different time and wavelength windows or from different modules
 via Frame Clock, Line Clock, and Pixel Clock pulses
 1 to 16

64	256	1024	4096
4096 x 4096	2048 x 2048	1024 x 1024	512 x 512
1024 x 1024	512 x 512	256 x 256	128 x 128

Operation Environment

Computer / operating system
 Bus connector
 Used PCI-ex slots
 Total power consumption
 Dimensions

PC Pentium, multi-core, >8GB RAM, Windows 10
 PCI-ex
 1
 approx. 12 W from +12V
 230 mm x 130 mm x 18 mm

Related Products

SPC-150N, SPC-150NX, SPC-150NXX TCSPC modules, HPM-100 GaAsP and GaAs hybrid detectors, DCC-100 pciex detector controller
 BDL-SMN ps diode lasers, BDS-SM, -SMY, -MM picosecond diode lasers

Related Literature

W. Becker, The bh TCSPC Handbook, 8th edition (2019), 950 pages, available on <https://www.becker-hickl.com>. Please contact bh for printed copies.
 The bh TCSPC Technique, Principles and Applications. Overview brochure, 27 pages. Available on <https://www.becker-hickl.com>

International Sales Representatives



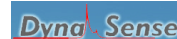
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