

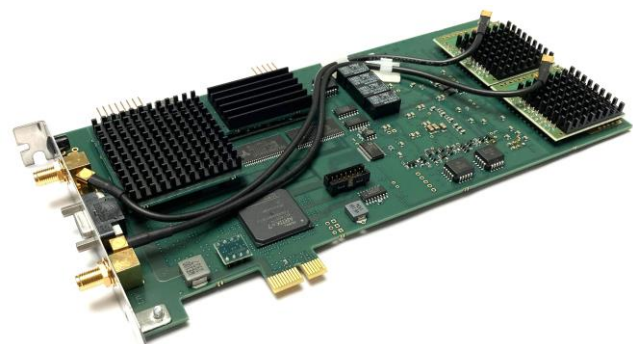
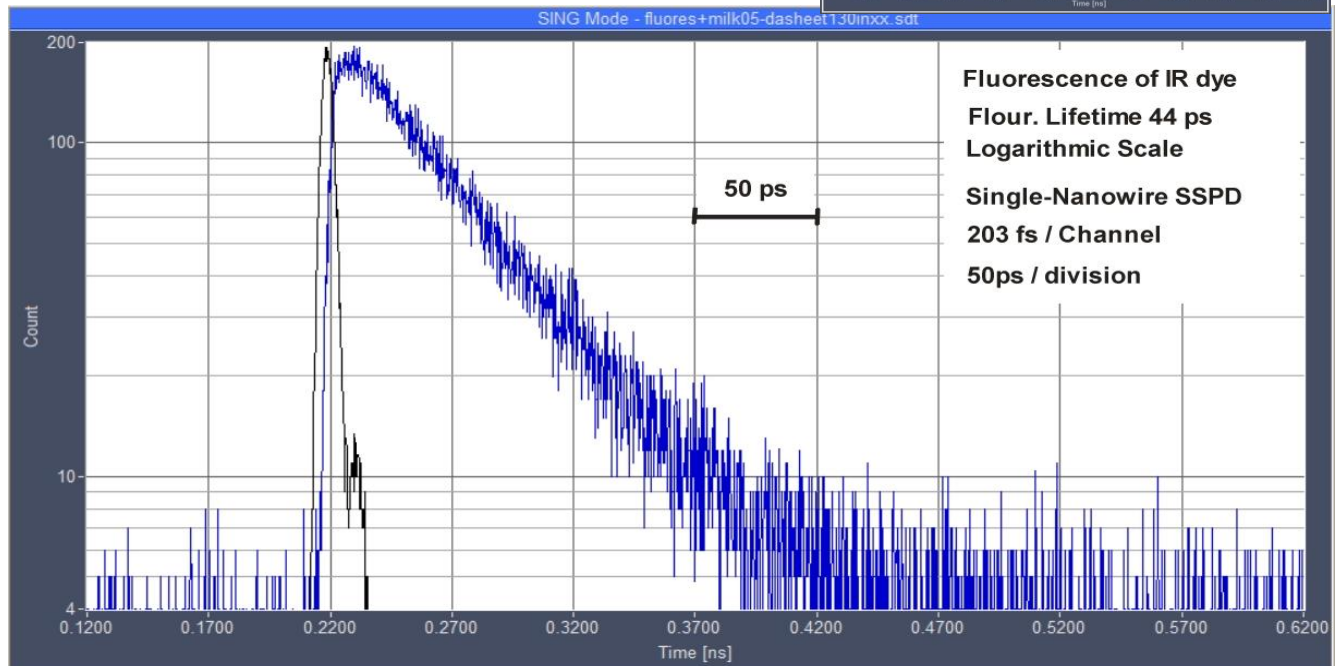
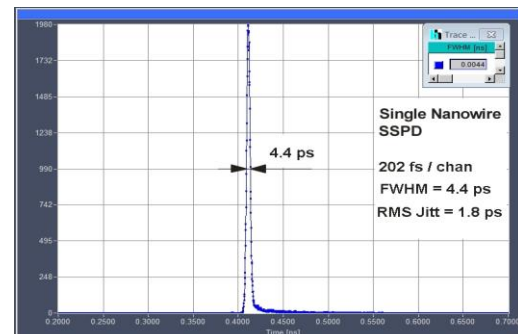
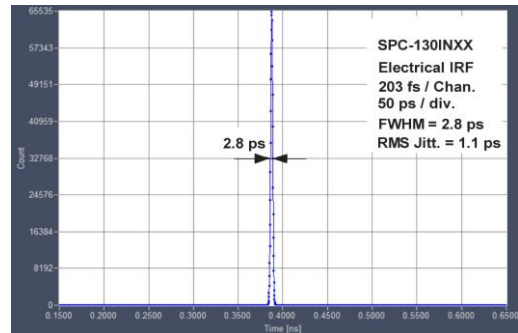


## Ultra-High Resolution Time-Correlated Single Photon Counting Module

### SPC-180NXX technology

- High-throughput PCI-Express interface
- Ultra-fast, ultra-stable timing electronics
- Electrical IRF width typ. 2.8 ps, FWHM
- Internal timing jitter 1.1 ps, RMS
- Time-channel width down to 203 fs
- Discriminator input bandwidth 4 GHz
- Recording-time interval 0.83 ns to 50 ns
- Photon distribution and parameter-tag modes
- Multi-detector / multi-wavelength capability
- Excitation-wavelength multiplexing
- Parallel operation of 2, 3 or 4 modules
- Laser repetition rates up to 150 MHz
- Dead time 80 ns
- Saturated count rate 12.5 MHz

- Ideal for superconducting NbN detectors (SSPDs)
- Ideal for ultra-fast hybrid detectors
- Ultra-high resolution fluorescence-lifetime experiments
- Photon correlation
- Anti-bunching experiments
- NIRS and fNIRS experiments at short distance
- Simultaneous multi-wavelength detection
- Simultaneous fluorescence / phosphorescence



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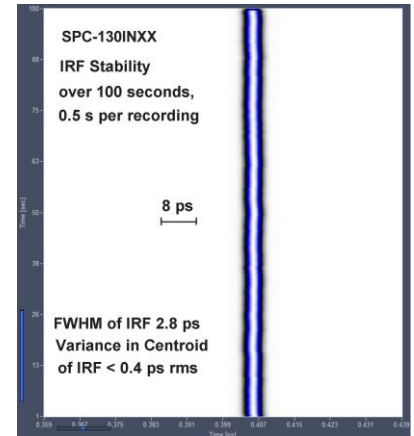
# SPC-130INXX

# TCSPC Module

## Photon Channel

Principle  
 Discriminator Input Bandwidth  
 IRF Width, FWHM  
 RMS Timing Jitter  
 Variance in Time of IRF Centroid  
 Optimum Input Voltage Range  
 Min. Input Pulse Width  
 Threshold  
 Zero Cross Adjust

Constant Fraction Discriminator (CFD)  
 4 GHz  
 < 3 ps, FWHM  
 < 1.1 ps, RMS  
 <0.4 ps RMS over 100 seconds  
 - 30 mV to - 500 mV  
 200 ps  
 0 to - 250 mV  
 - 100 mV to + 100 mV



## Synchronisation Channel

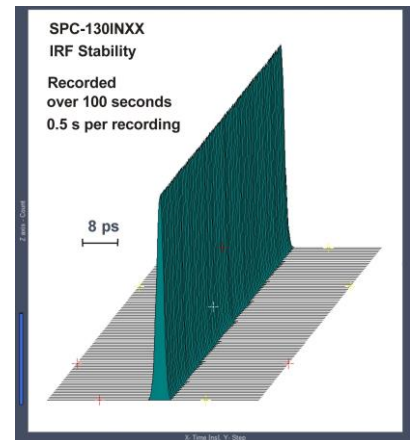
Principle  
 Discriminator Input Bandwidth  
 Optimal Input Voltage Range  
 Min. Input Pulse Width  
 Threshold  
 Frequency Range  
 SYNC Frequency Divider  
 Zero Cross Adjust

Constant Fraction Discriminator (CFD)  
 4 GHz  
 - 30 mV to - 500 mV  
 200 ps  
 0 to -250 mV  
 0 to 150 MHz  
 1 - 2 - 4  
 -100 mV to + 100 mV

## Time-to-Amplitude Converters / ADCs

Principle  
 TAC Range  
 Biased Amplifier Gain  
 Biased Amplifier Offset  
 Time Range incl. Biased Amplifier  
 Min. Time / Channel  
 ADC Principle  
 Diff. Nonlinearity, Electrical

Ramp Generator / Biased Amplifier  
 12.5 ns to 50 ns  
 1 to 15  
 0 to 50 % of TAC Range  
 0.83 ns to 99 ns  
 203 fs  
 50 ns Flash ADC with Error Correction  
 < 0.5 % RMS, typ. <1 % peak-peak



## Data Acquisition (Histogram Modes)

Method  
 Dead Time  
 Saturated Count Rate  
 Useful Count Rate  
 Max. Counts / Time Channel (Counting Depth)  
 Overflow Control  
 Collection Time  
 Display Interval Time  
 Repeat Time  
 Sequential Recording  
 Routing  
 Count Enable  
 Experiment Trigger

on-board multi-dimensional hardware histogramming process  
 80 ns, independent of computer speed  
 12 MHz  
 6 MHz  
 $2^{16}-1$   
 none / stop / repeat and correct  
 0.1 us to 100,000 s  
 10 ms to 100,000 s  
 0.1 us to 100,000 s  
 Unlimited recording by memory swapping  
 7 bit TTL / CMOS  
 1 bit TTL / CMOS  
 TTL / CMOS

## Data Acquisition (FIFO / Parameter-Tag Mode)

Method  
 Online Display  
 FCS Calculation  
 Number of Counts of Decay / Waveform Recording  
 Dead Time  
 Saturated Count Rate, Peak  
 Sustained Count Rate (Bus-transfer Limited)  
 Max. Counts / Time Channel (Counting Depth)  
 Output Data Format (ADC / Macrotime / Routing)  
 On-board FIFO Buffer Capacity (Photons)  
 Macro Timer Resolution, Internal Clock  
 Macro Timer Resolution, Clock from SYNC Input  
 Routing  
 External Event Markers  
 Experiment Trigger

Parameter-tagging of individual photons, continuous writing to disk  
 Decay function, FCS, Cross-FCS, PCH, MCS traces  
 Multi-tau algorithm, online calculation and online fit  
 unlimited  
 80 ns  
 12 MHz  
 5 MHz  
 unlimited  
 12 / 12 / 4 bit  
 $2 \cdot 10^5$   
 25 ns, 12 bit, overflows marked by MTOF entry in data stream  
 10 ns to 100 ns, 12 bit, overflows marked by MTOF entry in data stream  
 4 bit TTL / CMOS  
 4 bit, TTL / CMOS  
 TTL / CMOS

## Operation Environment

Computer / Operating System  
 Bus Connector  
 Used PCI-ex Slots  
 Total Power Consumption  
 Dimensions

PC Pentium, multi-core, >8GB RAM, Windows 10, Windows 11  
 PCI-ex  
 1  
 approx. 12 W from +12V  
 230 mm x 130 mm x 18 mm

## Related Products

SPC-130IN, SPC-130INX, SPC-180N, SPC-180NX, SPC-180INXX, SPC-150N, SPC-150NX, SPC-150NXX TCSPC modules, HPM-100-06 and -07 hybrid detectors  
 BDL-SMN ps diode lasers, BDS-SM, picosecond diode laser, DCS-120 multiphoton FLIM systems

## Related Literature

W. Becker, The bh TCSPC Handbook, 9th edition (2021), 950 pages, available on <https://www.becker-hickl.com>. Please contact bh for printed copies.  
 The bh TCSPC Technique, Principles and Applications. Overview brochure, 27 pages. Available on <https://www.becker-hickl.com>

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