



DDG-210

Digital Delay Generator

Digital Pulse / Delay Generator

Trigger Input

Synchronous Reference Output

6 Delayed Output Channels

Delay Resolution 1.25 ns

Pulse Width (Signal) from 10 ns to 2.5 ms

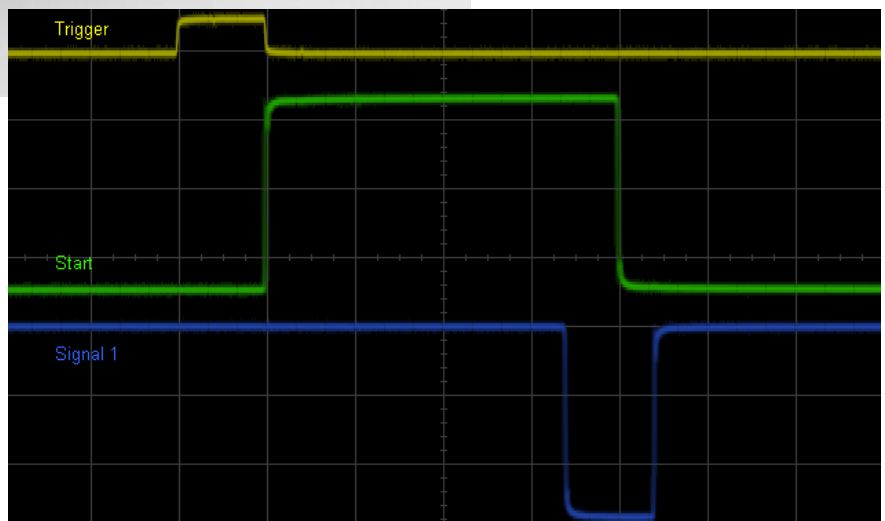
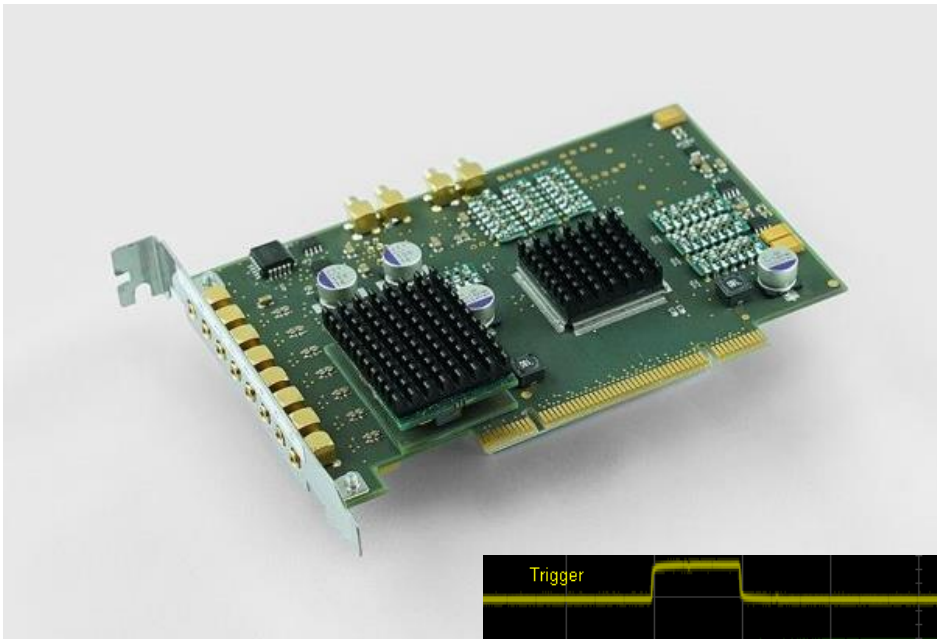
Maximum Cycle Time 42.9 s

Outputs TTL- / CMOS Compatible

ON/OFF Control of bh Diode Laser

Control of FLIM/PLIM Experiment

PCI Interface



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Digital Delay Generator

Trigger Input (Trigger)

Trigger Modes	none, each cycle, each sequence
Trigger Threshold	tuneable, -1 ... 1 V
Trigger Edge	rising or falling edge
Delay to Reference Output (Start)	50 ns
Max. Number of Cycles	4095 or endless

Reference Output (Start)

Pulse Period	30 ns to 42.9 s
Pulse Period Resolution	10 ns
Pulse Width	50 ns to 42.9 s
Pulse Width Resolution	10 ns
Output Type	Single-Ended TTL/CMOS
Output Impedance	50 Ohm
Drive Capability	2.5 V into 50 Ohm or 5 V open Circuit
Connector	MCX, 50 Ohm

Delayed Outputs (Signal 1 – 6)

Delay Range	50 ns to 42.9 s
Delay Resolution	1.25 ns
Delay Jitter	<50 ps
Output Polarity	H or L active, selectable
Output Impedance	50 Ohm
Drive Capability	2.5 V into 50 Ohm or 5 V open Circuit
Connectors	MCX, 50 Ohm
Pulses per Output	up to 64
Min.Pulse Distance	30 ns
Min. Pulse Width	10 ns
Max. Pulse Width	2.5 ms

Operation Environment

Computer / Operating System	PC Pentium, multi-core, >8 GB RAM, Windows 10, Windows 11
Bus Connector	PCI
Total Power Consumption	approx. 8 W from +5 V
Dimensions	148 mm x 97 mm x 23 mm

Related Literature

W. Becker, The bh TCSPC Handbook, 9th edition (2021). 950 pages, available on <https://www.becker-hickl.com>. Please contact bh for printed copies.

The bh TCSPC Technique, Principles and Applications. Overview brochure, 27 pages. Available on <https://www.becker-hickl.com>

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