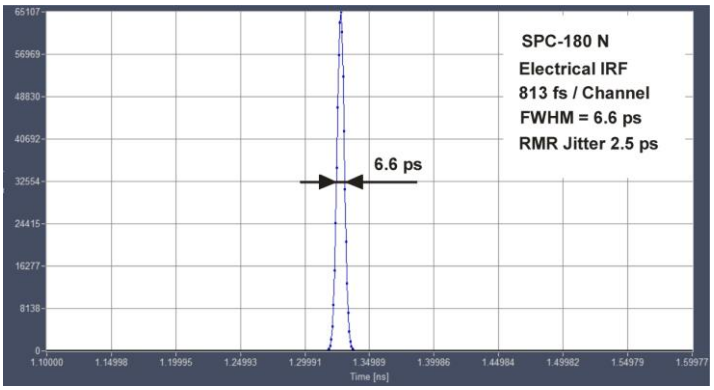
SPC-180N TCSPC / FLIM Module

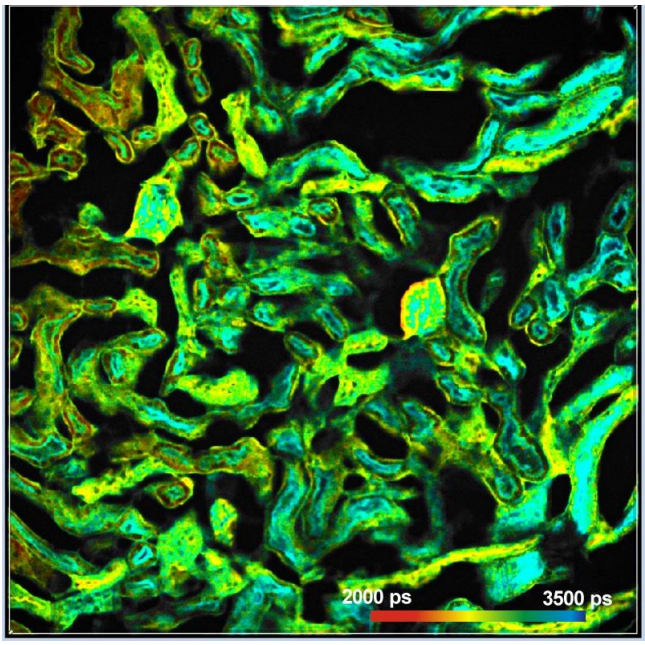
High-Resolution Time-Correlated Single Photon Counting Module

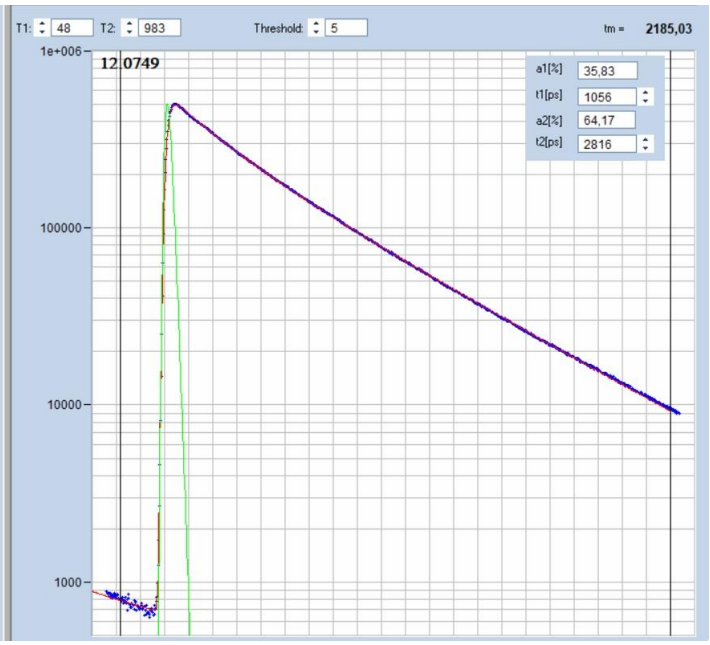
High-throughput PCI-Express interface
Ultra-fast, ultra-stable timing electronics
Electrical IRF width 6.6 ps FWHM
Internal timing jitter 2.5 ps RMS
Time-channel width down to 813 fs
Discriminator input bandwidth 4 GHz
Photon distribution and time/parameter-tag modes
Multi-detector / multi-wavelength capability
Excitation-wavelength multiplexing
Parallel operation of 2, 3 or 4 modules
Laser repetition rates up to 150 MHz
Dead time 80 ns
Saturated count rate 12.5 MHz

Fluorescence-decay experiments
Anti-bunching experiments
Single-wavelength FLIM, multi-wavelength FLIM
Fast-acquisition FLIM
Accumulated time-series FLIM
Simultaneous FLIM / PLIM
Mosaic FLIM



Metabolic imaging
Double-exponential FRET imaging
FLIM of fast physiological processes
Recording of Ca^{2+} transients
fNIRS and NIRS experiments
Single-molecule spectroscopy
Fluorescence correlation





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More than 28 years experience in TCSPC. More than 2500 TCSPC systems worldwide.

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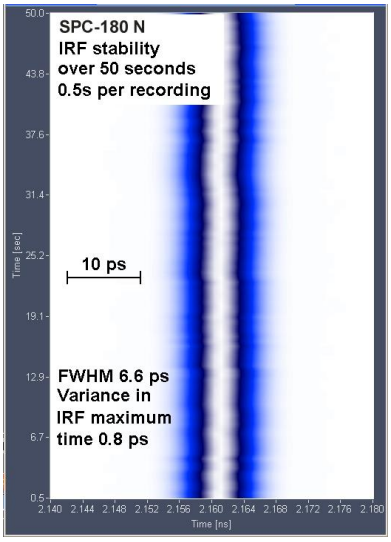

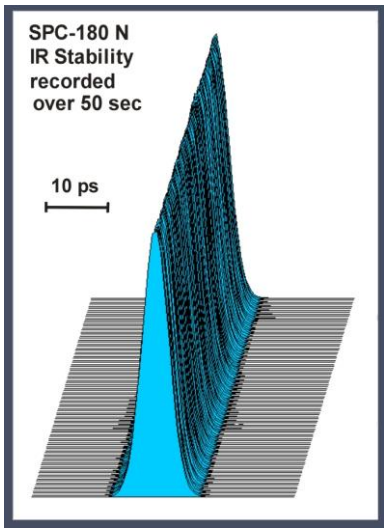

Photon Channel

Principle	Constant Fraction Discriminator (CFD)
Discriminator Input Bandwidth	4 GHz
IRF Width, FWHM	< 6.6 ps, FWHM
RMS Timing Jitter	< 2.5 ps, RMS
Variance in Time of IRF Centroid	<0.4 ps RMS over 100 seconds
Optimum Input Voltage Range	-30 mV to -500 mV
Min. Input Pulse Width	200 ps
Threshold	0 to -500 mV
Zero Cross Adjust	-100 mV to +100 mV

Synchronisation Channel

Principle	Constant Fraction Discriminator (CFD)
Discriminator Input Bandwidth	4 GHz
Optimal Input Voltage Range	-30 mV to -500 mV
Min. Input Pulse Width	200 ps
Threshold	0 to -500 mV
Frequency Range	0 to 150 MHz
SYNC Frequency Divider	1 - 2 - 4
Zero Cross Adjust	-100 mV to +100 mV

Time-to-Amplitude Converters / ADCs

Principle	Ramp Generator / Biased Amplifier
TAC Range	50 ns to 5 us
Biased Amplifier Gain	1 to 15
Biased Amplifier Offset	0 to 50 % of TAC Range
Time Range incl. Biased Amplifier	3.3 ns to 5 us
Min. Time / Channel	813 fs
ADC Principle	50 ns Flash ADC with Error Correction
Diff. Nonlinearity, Electrical	< 0.5 % RMS, typ. <1 % peak-peak

Data Acquisition (Histogram Modes)

Method	on-board multi-dimensional hardware histogramming process
Dead Time	80 ns, independent of computer speed
Saturated Count Rate	12 MHz
Useful Count Rate	6 MHz
Max. Counts / Time Channel (Counting Depth)	2^{16}-1
Overflow Control	none / stop / repeat and correct
Collection Time	0.1 us to 100,000 s
Display Interval Time	10 ms to 100,000 s
Repeat Time	0.1 us to 100,000 s
Sequential Recording	Unlimited recording by memory swapping
Synchronisation with Scanning	pixel, line and frame clocks from scanning device
Routing	7 bit TTL
Count Enable	1 bit TTL
Experiment Trigger	TTL

Data Acquisition (FIFO / Parameter-Tag Mode)

Method	Parameter-tagging of individual photons and continuous writing to disk
Online Display	Decay function, FLIM, FCS, Cross-FCS, PCH, MCS traces
FCS Calculation	Multi-tau algorithm, online calculation and online fit
Number of Counts of Decay / Waveform Recording	unlimited
Dead Time	80 ns
Saturated Count Rate, Peak	12 MHz
Sustained Count Rate (Bus-transfer Limited)	5 MHz
Max. Counts / Time Channel (Counting Depth)	unlimited
Output Data Format (ADC / Macrotime / Routing)	12 / 12 / 4 bit
On-board FIFO Buffer Capacity (Photons)	$2 \cdot 10^6$
Macro Timer Resolution, Internal Clock	25 ns, 12 bit, overflows marked by MTOF entry in data stream
Macro Timer Resolution, Clock from SYNC Input	10 ns to 100 ns, 12 bit, overflows marked by MTOF entry in data stream
Routing	4 bit TTL
External Event Markers	4 bit, TTL
Experiment Trigger	TTL

Data Acquisition, FIFO Imaging

Method	Buildup of images from time- and wavelength tagged data			
Online Display	up to 8 images in different time and wavelength windows or from different modules			
Synchronisation with Scanner	via Frame Clock, Line Clock, and Pixel Clock pulses			
Detector / Wavelength Channels	1 to 16			
Image Resolution, 64-bit SPCM Software				
No of Time Channels	64	256	1024	4096
No. of Pixels, 1 Detector Channel	4096 x 4096	2048 x 2048	1024 x 1024	512 x 512
No. of Pixels, 16 Detector Channels	1024 x 1024	512 x 512	256 x 256	128 x 128

Operation Environment

Computer / Operating System	PC Pentium, multi-core, >8GB RAM, Windows 10, Windows 11
Bus Connector	PCI-ex
Total Power Consumption	approx. 12 W from +12V
Dimensions	230 mm x 130 mm x 18 mm

Related Products

SPC-180NX, SPC-180NXX TCSPC Modules, SPC-150N, SPC-150NX, SPC-150NXX TCSPC modules
HPM-100 GaAsP and GaAs hybrid detectors, DCC-100PCIe detector controller
BDL-SMN ps diode lasers, BDS-SM, -SMY, -MM picosecond diode lasers, SPCImage NG data analysis software

Related Literature

W. Becker, The bh TCSPC Handbook, 9th edition (2021). 950 pages, available on https://www.becker-hickl.com. Please contact bh for printed copies.
The bh TCSPC Technique, Principles and Applications. Overview brochure, 27 pages. Available on https://www.becker-hickl.com

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